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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/031,326	02/26/1998	JOSEPH J. KARNIEWICZ	303.376US1	8474

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EXAMINER	
PHAN, THAI Q	
ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

NM

Office Action Summary	Application No. 09/031,326	Applicant(s) Joseph J. Karnlewicz
	Examiner Thai Phan	Art Unit 2123

-- Th MAILING DATE of this communication appears on th cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Jan 4, 2002

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-25 is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-25 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

This Office Action is response to applicant's remark, filed Jan. 04, 2002. Claims 1-25 are pending in this official action.

1. Acknowledgment has been made for the drawings correction.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Robinson et al., patent no. 5,524,244.

As per claims 1 and 9, Robinson anticipated method, design system with databases stored in memory, program product for populating parameters of cells or design configuration files (Abstract,"Summary of the Invention", col. 3, line 65 to col. 5, line 30) for use in circuit design environment and realization of silicon on chip design identical to the claimed invention. According to Robinson, the design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables

to the global variables in system files (col. 6, lines 21-36, col. 8, lines 41-67, col. 9, lines 1-12), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells (Figs. 3-12, col. 34, "Overview", col. 35, lines 1-28, col. 36, line 55 to col. 37, line 7, col. 53, lines 44-55, cols. 50-56, 59-62 for example).

As per claims 2-3 and 10-11, Robinson disclosed local files include inherent file from source files, instance files, data files, etc. (Figs. 3-12).

As per claim 4, Robinson disclosed master files in hierarchical design acting as initial version of a corresponding local file for design, modification, increment compilation, etc.

As per claim 5, Robinson disclosed file or clean sheet file for containing design rules for a plurality of cells for coordinated design as claimed.

As per claim 6, Robinson disclosed file extraction and related variable extraction for design and update design.

As per claims 7-8, Robinson anticipated the design display in local host for display interactively interface.

As per claim 12, Robinson disclosed file update including update global file for coordinate process.

As per claim 13, Robinson anticipated local display in local user workstation for the design process.

As per claim 14, Robinson disclosed computer program in concurrent with design program for circuit design process as claimed.

As per claim 15, Robinson anticipates method and system of workstations, databases, shared memory, etc. for populating parameters of cells (Abstract, Figs. 3-12, cols. 4-5, 59-62, for example) for use in circuit design, programming design, silicon on chip design etc. environment identical to the claimed invention. According to Robinson, the design apparatus includes local user work stations, central workstations, global files of global variables and design database, system memory for sharing between users for distribution processing (cols. 4, 5, col. 9, lines 12-23), a plurality of local files, each relating a plurality of local variables to the global variables (cols. 4-5, col. 35, lines 1-28, cols. 50-56, 60-64, for example), and a plurality of instance cells being programmable, each cell corresponding to a local file of subcircuit blocks and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the cells (Figs. 3-12, cols. 4-5, cols. 34-36 for overviews for design methodology, col. 53, lines 44-55, col. 54-56, 60-64, etc.) or updating variables in configuration files or local files by reading from the global file value of global variables to which the local variables of the local file correspond for complete design as claimed.

Similarly, claims 16-21 are also rejected due to its similarities to claims 2-8 and claims 11-14.

As per claim 22, Robinson anticipated method, design system with databases stored in memory, program product for populating parameters of cells (Abstract,"Summary of the

Invention", col. 3, line 65 to col. 5, line 30) for use in circuit design environment identical to the claimed invention. According to Robinson, the design apparatus includes global files for global variables and design data relating to layout and connectivity data of the functional block, a plurality of local files, each relating a plurality of local variables to the global variables (col. 6, lines 21-36, col. 8, lines 41-67, col. 9, lines 1-12, col. 34, "Overview", col. 35, lines 1-28, cols. 50-56, 60-64, etc.), and a plurality of cells, each cell corresponding to a configuration file or a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells (Figs. 3-12, cols. 59-62 for example).

As per claims 23-24, Robinson anticipated inherent design file, and instance file in the design database.

As per claim 25, Robinson anticipated design framework for use in the chip design process. Such design framework could be used as CADENCE functional design system as claimed.

Response to Arguments

4. Applicant's arguments filed Jan. 04, 2002 have been fully considered but they are not persuasive.

In response to applicant's argument Robinson does not teach programmable design cells (page 2, last paragraph), the examiner disagrees with. Robinson disclosed method and system for design integrated circuits such as programmable real time signal processor (Abstract). The circuit

design includes a plurality of circuit blocks or cells (col. 34, lines 17-27), defining parameters for design circuit functional blocks, generating configuration files for parameterized functional blocks (col. 34, col. 35, lines 10-39), and layout designing for the chip using OrCAD (col. 36, col. 83, lines 47-50).

In response to applicant's argument Robinson does not relating local cell parameters to a global file for update in layout of element blocks of a hierarchical design or structure (page 3, paragraph 1), the examiner disagrees with applicant argument. As Robinson disclosure, the design method and system is for designing integrated circuit hierarchically (col. 53, lines 44-55, cols. 56, 59-62). The design method required update program for update set of parameters of a design cell or instance cell by relating local parameters of a local file for the design cell a global file of global variables relating to layout or schematic diagram to complete the design and because of design hierarchy as shown in col. 34, "Overview", col. 53, lines 44-55, cols. 56, 59-62 for example

In response to applicant's argument Robinson fails to show computer program for circuit design and implementation (page 3, paragraph 2), the examiner disagrees with. Robinson disclosed circuit design automation. The design automation process required a software program for controlling and designing circuit as disclosed in col. 2, lines 39-47, col. 4, "Summary of the Invention", cols. 34-36, for "Overview", cols. 6-12, for detail architecture of the design environment.

In response to applicant's argument Robinson fails to "updating a set of parameter ..." (page 3, paragraph 3), the examiner disagrees with. Robinson disclosure, the design method and

system is for designing integrated circuit hierarchically (col. 53, lines 44-55, cols. 56, 59-62). The design method required update program for update set of parameters of a design cell or instance cell by relating local parameters of a local file for the design cell to a global file of global variables relating to layout or schematic diagram to complete the silicon on chip design and because of design hierarchy as shown in col. 34, "Overview", col. 36, line 55 to col. 37, line 17, col. 53, lines 44-55, cols. 56, 59-62.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Patent no. 6,026,226, issued to Heile et al., Feb. 2000

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this final action should be mailed to:

Box AF

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for Formal communications; please mark "EXPEDITED PROCEDURE"),

Or:

(703) 746-7239 (for Official Fax communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

February 18, 2002

DR. HUGH M. JONES
PATENT EXAMINER
ART UNIT 2123